



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,875	06/22/2001	Natsuki Kushiyama	81790.0204	8040

26021 7590 12/02/2004

HOGAN & HARTSON L.L.P.  
500 S. GRAND AVENUE  
SUITE 1900  
LOS ANGELES, CA 90071-2611

EXAMINER
----------

SHARON, AYAL I

ART UNIT	PAPER NUMBER
----------	--------------

2123

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/887,875

Applicant(s)

KUSHIYAMA, NATSUKI

Examiner

Ayal I Sharon

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☒ Claim(s) 1-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1,4,5,6</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Introduction***

1. Claims 1-22 of U.S. Application 09/887,875 filed on 06/21/2001 are presented for examination. The application claims priority to Japanese Application 2000-188857, filed on 06/23/2000.
2. The Examiner has taken into account the findings of the Japanese Patent Office in its Office Action regarding the priority case, Japanese Application 2000-188857, which the Applicant submitted for Examiner's review on 10/24/1003.

### ***Claim Objections***

3. Claims 1-22 objected to because of the following informalities: terms such as VREF<sub>n-1</sub> would be more legible if written using parenthesis, e.g. VREF(n-1), or with subscript, e.g. VREF<sub>n-1</sub>, or some other format. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2123

5. The prior art used for these rejections is:

Japanese Patent Application KOKAI Publication No. 11-97628, published 04/09/1999. (Henceforth referred to as "**Reference 1**").

**6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Reference 1.**

7. In regards to Claim 1, Reference 1 teaches the following limitations for the situation where wherein  $n = 2$ :

1. A semiconductor integrated circuit comprising:

a reference potential conversion circuit which is supplied with  $n-1$  ( $n$  is 2 or larger natural number) external reference potentials ( $V_{REF1}$ ,  $V_{REF2}$ , ...,  $V_{REFn-1}$ ) and converts external reference potentials to generate  $n-1$  internal reference potentials ( $V_{REFint1}$ ,  $V_{REFint2}$ ,  $V_{REFintn-1}$ ) differing from external reference potentials and having a relationship with regard to the  $n-1$  external reference potentials, and

an input circuit which is supplied with said internal reference potential ( $V_{REFint1}$ ,  $V_{REFint2}$ ,  $V_{REFintn-1}$ ) as reference potentials, is supplied with  $n$  values of data signals expressed by potentials, and compares a data signal and a reference potential to output a determination result.

See especially FIGS. 1--4 and the explanations (paragraphs [0045] to [00651]), in particular:

A semiconductor integrated circuit including:

reference potential conversion circuits ("internal voltage generating circuits 21, 23,...") which output a plurality of internal reference potentials (voltages " $V_{ref3}$ " generated by "internal voltage generating circuits 21, 23, ..." in FIGS. 1 and 4), respectively, based on an external reference potential (voltage " $V_{ref2}$ " generated by "reference voltage generating circuit 31" in FIGS. 1 and 3); and

input circuits (designed by reference numerals 11, 13, 15, 17 and 19, and whose circuit diagram is shown in FIG. 2) which output judgment results (" $V_{OUT}$ ") of comparison/judgment of input signals (" $V_{IN}$ " and " $eF3$ ") using the output potentials (" $V_{ref3}$ ") from the reference potential conversion

circuits as reference potentials.

In regards to when  $n \geq 3$ , Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B)

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. The prior art used for these rejections is as follows:

- a. Japanese Patent Application KOKAI Publication No. 11-97628, published 04/09/1999. (Henceforth referred to as "**Reference 1**").
- b. Japanese Patent Application KOKAI Publication No. 11-204740, published 11/09/1999. (Henceforth referred to as "**Reference 2**").
- c. Japanese Patent Application KOKAI Publication No. 11-312785, published 07/30/1999. (Henceforth referred to as "**Reference 3**").
- d. Japanese Patent Application KOIIAI Publication No. 2000-68458, published 03/03/2000. (Henceforth referred to as "**Reference 4**").
- e. Japanese Patent Application KOKAI Publication No. 5-29464, published 02/05/1993. (Henceforth referred to as "**Reference 5**").

Art Unit: 2123

10. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

**11. Claims 2, 5-6 and 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reference 1 in view of Reference 2.**

12. In regards to Claim 2,

2. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials ( $V_{REF1}$ ,  $V_{REF2}$ ,  $V_{REFn-1}$ ) and said internal reference potentials ( $V_{REFint1}$ ,  $V_{REFint2}$ ,  $V_{REFintn-1}$ ) is expressed by  $V_{REFintn-1} = V_{REFn-1} + A$  ( $n$  is 2 or larger natural number and  $A$  is a rational number except 0).

Reference 1 teaches a "reference potential conversion circuit."

However, Reference 1 does not expressly teach the increase / amplification of the external reference voltage.

Reference 2, on the other hand, expressly teaches (Fig. 4 and the explanations in paragraphs [0052] to [00571]) the use of an operational amplifier (45) and a resistance element (11) (in other words, a circuit whose structure is the same as that of the circuit described in FIG. 9 of the present application) to produce an output reference voltage larger than an input reference voltage.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of Reference 2, because it was old and well known at the time the invention was made.

13. In regards to Claim 5,

5. The semiconductor integrated circuit according to claim 1, further comprising a storage circuit for

Art Unit: 2123

holding data of a plurality of bits, and wherein  
said relationship between said external reference  
potentials (VREF1, VREF2, ..., VREFn-1) and said  
internal reference potentials (VREFint1, VREFint2,  
VREFintn-1) is changed based on data of a plurality of  
bits stored in said storage circuit.

Reference 1 does not disclose that the conversion operation of the voltage  
conversion circuit described in FIG. 4 is controlled based on data stored in some  
kind of storage means.

Reference 2, on the other hand (see Fig.4, "register 44") teaches such an  
apparatus.

It would have been obvious to one of ordinary skill in the art at the time the  
invention was made to modify the teachings of Reference 1 with those of  
Reference 2, because it was common and well known in the art to control  
conversion operation of a voltage conversion circuit based on data stored in a  
storage means.

14. In regards to Claim 6,

6. The semiconductor integrated circuit according  
to claim 5, wherein  
said storage circuit for holding data of a  
plurality of bits is a one-time programmable storage  
circuit, and  
said relationship between said external reference  
wherein potentials (VREF1, VREF2, ..., VREFn-1) and said  
internal reference potentials (VREFint1, VREFint2, ...,  
VREFintn-1) is changed based on data of a plurality of  
bits stored in said storage circuit.

Reference 1 does not disclose that the conversion operation of the voltage  
conversion circuit described in FIG. 4 is controlled based on data stored in some  
kind of storage means.

Reference 2, on the other hand (see Fig.4, "register 44") teaches such an apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of Reference 2, because it was common and well known in the art to control conversion operation of a voltage conversion circuit based on data stored in a storage means.

15. In regards to Claim 10, Reference 1 teaches the following limitations:

10. The semiconductor integrated circuit according to claim 5, wherein  
said storage circuit for holding data of a plurality of bits is a re-programmable storage circuit and  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1), and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said storage circuit.

Reference 1 teaches (See Fig.2, "input circuit 11") an input circuit that performs a comparison operation at edge timing of clock signal " $\Phi$ ".

16. In regards to Claim 11, Reference 1 teaches the following limitations:

11. The semiconductor integrated circuit according to claim 10, wherein  
said storage circuit includes a semiconductor memory circuit for specifying data of a plurality of bits to be held, and  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said semiconductor memory circuit.

Examiner finds that the teaching of Reference 1 pertains to a semiconductor memory circuit (see abstract), and that the input circuit that

performs a comparison operation (See Fig.2, "input circuit 11") inherently "specifies data" for "a plurality of bits to be held".

17. In regards to Claim 12, Reference 1 teaches the following limitations:

12. The semiconductor integrated circuit according to claim 10, wherein  
said storage circuit includes a register for specifying data of a plurality of bits to be held, and  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said register.

Examiner finds that the teaching of Reference 1 pertains to a semiconductor memory circuit (see abstract), and that the input circuit that performs a comparison operation (See Fig.2, "input circuit 11") for "a plurality of bits to be held" corresponds to a register.

18. In regards to Claim 13, Reference 1 teaches the following limitations:

13. The semiconductor integrated circuit according to claim 1, further comprising a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and wherein  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

See MPEP §2144.04 (VI)(B).

19. In regards to Claim 14, Reference 1 teaches the following limitations:

14. The semiconductor integrated circuit according to claim 13, further comprising a selection circuit for selecting said first storage circuit or said second

Art Unit: 2123

storage circuit, and wherein  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

In regards to when multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B).

20. Claims 15 are rejected on the same grounds as Claim 14, because they claim the same limitations.

21. In regards to Claim 16, Reference 1 teaches the following limitations:

16. The semiconductor integrated circuit according to claim 5, wherein said input circuit compares an input data signal with the reference potential having n-1 values at the timing of a clock signal's leading and trailing edge or either edge and outputs a comparison result.

Reference 1 teaches (See Fig.2, "input circuit 11") an input circuit that performs a comparison operation at edge timing of clock signal " $\Phi$ ".

22. Claims 17-18 are rejected on the same grounds as Claim 16, because they claim the same limitations.

**23. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reference 1 in view of Reference 3.**

24. In regards to Claim 3, Reference 1 does not expressly teach the following limitations:

3. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials

Art Unit: 2123

(VREFint1, VREFint2, ... VREFintn-1) is expressed by  
 $VREFintn-1 = B \times VREFn-1$  (n is 2 or larger natural  
number and B is a rational number except 0).

On the other hand, Reference 3 (see Fig.1) teaches a voltage  
dividing circuit comprising resistance elements R1, R2, R3 and R4 producing  
a desired voltage "VREFA" from a "reference potential".

It would have been obvious to one of ordinary skill in the art at the time the  
invention was made to modify the teachings of Reference 1 with those of  
Reference 3, because it was old and well known to employ a voltage dividing  
circuit that uses resistance elements to produce, based on a reference voltage, a  
voltage different from the reference voltage..

**25. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over  
Reference 1 in view of Reference 2 and further in view of Reference 3.**

26. In regards to Claim 4, Reference 1 does not expressly teach the following

limitations:

4. The semiconductor integrated circuit according  
to claim 1, wherein said relationship between said  
external reference potentials (VREF1, VREF2, ...,  
VREFn-1) and said internal reference potentials  
(VREFint1, VREFint2, ..., VREFint1) is expressed by  
 $VREFintn-1 = C \times VREFn-1 + D$  (n is 2 or larger natural  
number and, C and D are rational numbers except 0).

Examiner interprets that claim 4 is based on the description in paragraph  
[0048] in the specification of the present application. In other words, it is  
considered that the "reference potential conversion circuit" recited in claim 4 of  
the present application is a circuit produced by combining the conversion circuits  
disclosed in FIGS. 2 and 9 of the present application.

However, as stated above, the circuits disclosed in FIGS. 2 and 9 of the present application are circuits of well-known art, as they are described in References 3 and 2, respectively.

It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the teachings of Reference 1 with the teachings of References 2 and 3, respectively, because the teachings of References 2 and 3 were old and well known.

**27. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reference 1 in view of Reference 2 and further in view of Reference 4.**

28. In regards to Claim 7, Reference 1 teaches the following limitations:

7. The semiconductor integrated circuit according to claim 6, wherein  
said storage circuit includes a laser beam blown type fuse for specifying data of a plurality of bits to be held depending on whether a laser beam disconnects the fuse, and wherein  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said laser beam blown type fuse.

Reference 1 teaches most of the limitations of the claim (see Figs. 1-4; especially "internal voltage generating circuits 21, 23, ..."), however, Reference 1 does not expressly teach that the conversion operation of the voltage conversion circuit described in Fig. 4 is controlled based on data stored in some kind of storage means.

Reference 2, on the other hand, teaches (see Fig. 4, "register 44") the common technique of conversion operation by a voltage conversion circuit based on data stored in a storage means.

Moreover, Reference 4 teaches (see Fig. 2 and paragraphs [0036] and [0043]), it is a well-known technique to employ, as a storage means, a storage means formed using a fuse that is blown by laser light.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of References 2 and 4, respectively, because it was old and well known to employ a storage means formed using a fuse like the one described in reference 4 instead of the "register 44" in FIG. 4 of reference 2.

**29. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reference 1 in view of Reference 2 and further in view of Reference 4 and further in view of Reference 5.**

30. In regards to Claim 8, Reference 1 does not expressly teach the following limitations:

8. The semiconductor integrated circuit according to claim 6, wherein  
    said storage circuit includes an electric current blown type fuse for specifying data of a plurality of bits to be held depending on whether an electric current disconnects the fuse, and  
    said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said electric current blown type fuse.

On the other hand, Reference 2 (see Fig.9 and col.8) and Reference 5 (see Figs.4-6 and Reference 5) teach the use of a "current-blowout-type fuse" or an "insulating-film-destruction-type fuse" as a fuse.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of References 2 and 5, respectively, because it is old and well known to "current-blowout-type fuse" or an "insulating-film-destruction-type fuse" as a fuse.

31. In regards to Claim 9, Reference 1 does not expressly teach the following limitations:

9. The semiconductor integrated circuit according to claim 6, wherein  
said storage circuit includes a dielectric film breakdown type fuse for specifying data of a plurality of bits to be held depending on whether a voltage breakdowns a dielectric film of the dielectric film breakdown type fuse, and  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said dielectric film breakdown type fuse.

On the other hand, Reference 2 (see Fig.9 and col.8) and Reference 5 (see Figs.4-6 and Reference 5) teach the use of a "current-blowout-type fuse" or an "insulating-film-destruction-type fuse" as a fuse.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of References 2 and 5, respectively, because it is old and well known to "current-blowout-type fuse" or an "insulating-film-destruction-type fuse" as a fuse.

Art Unit: 2123

**32. Claims 19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reference 1 in view of Official Notice.**

33. In regards to Claim 19, Reference 1 teaches the following limitations:

19. A semiconductor apparatus system, comprising:

a plurality of semiconductor integrated circuits which is mounted on said motherboard and includes a reference potential conversion circuit connected to said external reference signal line, supplied with  $n-1$  ( $n$  is 2 or larger natural number) external reference potentials ( $VREF1, VREF2, \dots, VREFn-1$ ), and generating other potentials ( $VREFint1, VREFint2, \dots, VREFintn-1$ ) differing from said external reference potentials and further includes an input circuit supplied with output potentials ( $VREFint1, VREFint2, \dots, VREFintn-1$ ) from said reference potential conversion circuit as reference potentials, supplied with a data signal from said data signal line, comparing the input data signal with reference potentials having  $n-1$  values for determination, and generating a determination result.

See especially FIGS. 1--4 and the explanations (paragraphs [0045] to [0065]), in particular:

A semiconductor integrated circuit including:  
reference potential conversion circuits ("internal voltage generating circuits 21, 23,...") which output a plurality of internal reference potentials (voltages "Vref 3" generated by "internal voltage generating circuits 21, 23, ..." in FIGS. 1 and 4), respectively, based on an external reference potential (voltage "Vref2" generated by "reference voltage generating circuit 31" in FIGS. 1 and 3); and

input circuits (designed by reference numerals 11, 13, 15, 17 and 19, and whose circuit diagram is shown in FIG. 2) which output judgment results ("VOUT") of comparison/judgment of input signals ("VIN" and "eF3") using the output potentials ("Vref3") from the reference potential conversion circuits as reference potentials.

In regards to when  $n \geq 3$ , Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP

§2144.04 (VI)(B)

However, Reference 1 does not expressly teach the following limitation:

a motherboard including an input/output terminal section and a data signal line and an external reference signal line connected to this input/output terminal section, and

Official Notice is given that it was old and well known at the time the invention was made to place circuits on motherboards, and laying the input/output terminal section and signal lines on the motherboard.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Reference 1 with those of Official Notice, because some circuits need to be implemented in the form of a motherboard.

34. In regards to Claim 21, Reference 1 teaches the following limitations:

13. The semiconductor integrated circuit according to claim 19, wherein  
said semiconductor integrated circuit further comprises a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and wherein  
said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

See MPEP §2144.04 (VI)(B).

35. In regards to Claim 22, Reference 1 teaches the following limitations:

14. The semiconductor integrated circuit according to claim 19, wherein  
said semiconductor integrated circuit further comprises a selection circuit for selecting said first storage circuit or said second storage circuit, and wherein

Art Unit: 2123

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

See MPEP §2144.04 (VI)(B).

**36. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over**

**Reference 1 in view of Official Notice.**

37. In regards to Claim 20,

20. The semiconductor apparatus system according to claim 19, wherein  
said semiconductor integrated circuit further comprises a storage circuit for holding data of a plurality of bits, and  
said relationship between said external reference potentials (VREF1, VREF2 ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, VREFintn-1) is changed based on data of a plurality of bits stored in said storage circuit.

Reference 1 does not disclose that the conversion operation of the voltage conversion circuit described in FIG. 4 is controlled based on data stored in some kind of storage means.

Reference 2, on the other hand (see Fig.4, "register 44") teaches such an apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of Reference 2, because it was common and well known in the art to control

Art Unit: 2123

conversion operation of a voltage conversion circuit based on data stored in a storage means.

***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

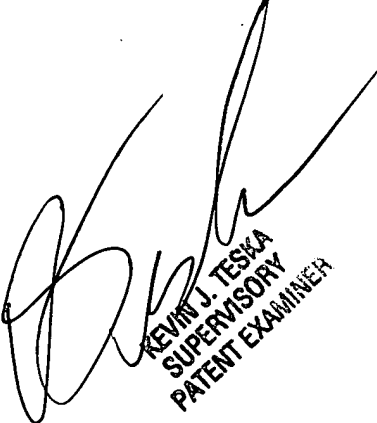
Director of Patents and Trademarks  
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

November 24, 2004



KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER